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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				FILING DATE: April 14, 2005	CONFIRMATION NO.: 5057
				APPLICANT: Laurent Regnier	
				GROUP ART UNIT: 2113	EXAMINER: M.C. Maskulinski
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U.S. PATENT DOCUMENTS

Examiner's Initials #	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or Issue of Cited Document MM-DD-YYYY
		Number	Kind Code		

FOREIGN PATENT DOCUMENTS

Examiner's Initials #	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/Country	Number	Kind Code			
		JP	11-306044		Norishige et al (w/English Translation)	11/05/1999	
		JP	2-244235		Kyoichi (w/English Abstract)	09/28/1990	
		JP	61-282944		Yasuhide (w/English Abstract)	12/13/1986	
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OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner's Initials #	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)
		The Nexus 5001 Forum™ Standard for a Global Embedded Processor Debug Interface, IEEE-ISTO 5001™, December 15, 1999, Section 4, page 13 and Section 6, pages 51, 59, 65 and 67-	

EXAMINER:	DATE CONSIDERED:
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* a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. __, filed __, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

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